BROADBAND HIGH-EFFICIENCY MMIC POWER AMPLIFIERS USING ION-IMPLANTED MESFET TECHNOLOGY*

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ABSTRACT

Broadband high-efficiency MMIC amplifiers had been designed and fabricated using ion-implanted MESFET technology. In the 7.5 to 18 GHz bandwidth, the amplifier has demonstrated a power-added efficiency of 15 to 34 percent, averaging greater than 20 percent. The output power is about 24 dBm at 1-dB compression and 26 dBm at 2-dB compression.

INTRODUCTION

There has been a large effort to develop monolithic power amplifiers with more than an octave bandwidth for electronic warfare applications. The broadband performance was achieved either by distributed amplifiers (1-3) or by conventional lossy-match or feedback amplifiers (4-6). Although up to about 2-watt power output had been achieved (4), the amplifier's power-added efficiency is low, typically less than 15 percent. In this paper, we present the design, fabrication, and performance of a broadband high-efficiency MMIC amplifier with an output power of 26 dBm. In the bandwidth of 7.5 to 18 GHz the amplifier's power-added efficiency is 15 percent minimum, 34 percent maximum, and averaging greater than 20 percent.

The amplifier circuit was fabricated using a selective ion-implantation technology with optical lithography. The process is highly reproducible and is suitable for MMIC production. Based on the result of the first few wafers, the dc yield is about 30 percent.

AMPLIFIER DESIGN

The goal for the amplifier design was 20 percent power-added efficiency, 0.5-watt output power, 6 to 18 GHz bandwidth, and 4-dB power gain minimum. To meet the design goal, a 1.2-mm Ku-band device was selected for the amplifier design. The device was characterized under a small-signal condition to determine its equivalent circuit elements and the output conductance was than modified based on the large-signal load-pull measurement. Since efficiency and power are our top priorities, we employed reactive matching for both input and output. The complete amplifier circuit is then optimized for flat gain.

A photograph of the completed MMIC amplifier is shown in Figure 1. Both lumped and distributed elements were used to realize the matching network. MOM capacitors were used as the bypass as well as the output tuning capacitors. At the gate bias line a 50-ohm resistor was employed as the stabilizing resistor. In addition, the low-impedance line transformer was equally splitted and isolation resistors added to suppress the potential odd-mode excitation. Probe pads were also included to allow for the on-wafer characterization. The finished chip size is 5 mm x 1.5 mm.

DEVICE AND MMIC FABRICATION

The fabrication procedure generally followed the Hughes' standard ion-implanted process for MMIC power amplifiers (7). It started with Si implant to form the active channel, followed by a capless anneal at 890°C. After mesa etch and source/drain ohmic formation, a proton isolation implant was performed. The 0.5-μm gate was then defined using contact lithograph and chemical recess etch. The process continued with a TaN thin film resistor, MOM capacitor formation, Si_3N_4 passivation, and airbridge plating to complete the front-side process. The entire process was completed with back-side thinning, via hole etching, and back metallization.

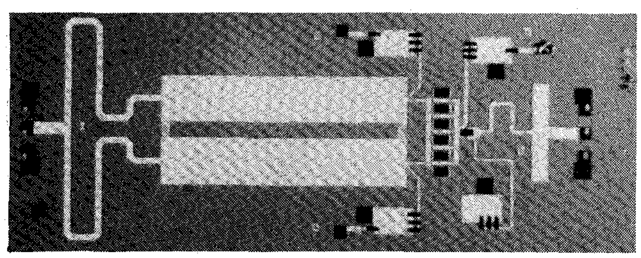

Figure 1 Photograph of a 6-18 GHz single-stage MMIC amplifier.

* This work is supported by a contract with the Naval Research Laboratory (Contract No. N00014-86-C-2568) under the guidance of Dr. K. Sleger.

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In the present work, the implant and gate-recess conditions were specially optimized to meet the efficiency, power, and frequency requirements, in order of priority. The ohmic metal was AuGe/Ni/Au, while the gate and overlay metal used Ti/Pt/Au. Via holes, etched with RIE technology, were used for source bypass capacitor groundings. Devices were processed both with and without Si_3N_4 passivation. No significant differences were observed in performance.

MEASURED PERFORMANCE

After fabrication, the amplifier was first characterized on-wafer for its small-signal performance. The on-wafer testing system consists of an HP8510B vector network analyzer integrated with a Cascade probe station. With the precision on-wafer calibration standards, the measured results represent the true response of the amplifier without the packaging effect from the conventional test jig. Based on the six wafers that were successfully fabricated and tested, the dc yield is about 30 percent. The small-signal performance of the amplifier shows about 6.5 dB gain from 7.5 to 18 GHz.

For power testing, the amplifier chip is diced and packaged in a test fixture with APC-7 input/output connectors. Bond wires are used to connect the chip to the 50-ohm microstrip lines on 25-mil alumina substrates. Figure 2 presents the measured output power as a function of frequency with the input power as the parameters. Observing at the low input power level, we notice that the amplifier has been slightly detuned by the fixture package to have a more pronounced gain ripple. Nevertheless, the power performance of the amplifier shows 24 dBm at 1-dB compression and 26 dBm at 2-dB compression. The associated power-added efficiency lies between a minimum of 15 percent and a maximum of 34 percent as shown in Figure 3. The averaged power-added efficiency across the band is greater than 20 percent. At the midband from 10 to 13.5 GHz, the amplifier has produced 26 to 27 dBm with a power-added efficiency of 26 to 34 percent.

CONCLUSION

Broadband high-efficiency MMIC amplifiers have been designed and fabricated using an ion-implanted MESFET technology. Octave bandwidth MMIC amplifiers with a power-added efficiency greater than 20 percent become possible using a production technology. The amplifier will be a useful building block in electronic warfare applications.

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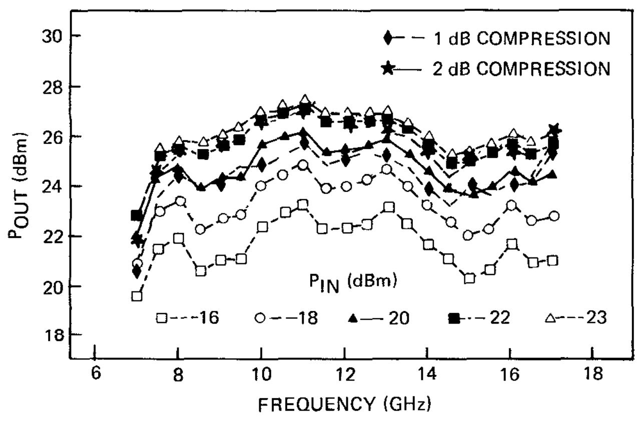

Figure 2 Output power performance of the 6-18 GHz MMIC amplifier.

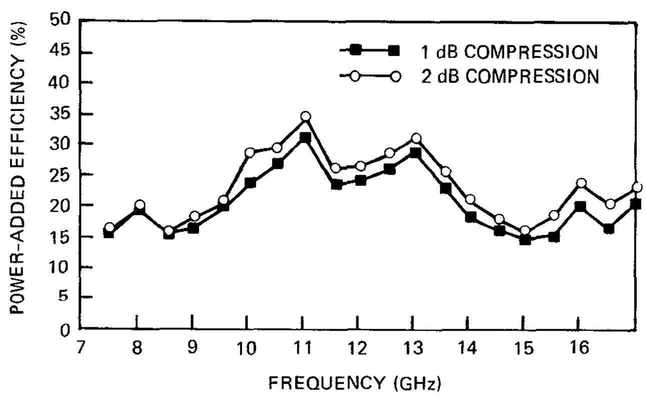

Figure 3 Power-added efficiency performance of the 6-18 GHz MMIC amplifier.